Remarks

As stated above, the applicants appreciate the Examiner's thorough examination of the subject application and request reexamination and reconsideration of the subject application in view of the preceding amendments and the following remarks.

The Examiner rejects claims 1-3 and 7-8, under 35 USC §103(a), based upon the combination of the teaching of Kobayashi (U.S. Patent No. 6,373,346, hereinafter Kobayashi) and Larson (U.S. Patent No.: 5,767,704, hereinafter Larson).

Applicants claim (in currently amended claim 1):

> 1. (Currently Amended) A laser driver circuit comprising: an input stage to receive an input signal; a limiting amplifier to generate a pulse data output signal in response to the input signal, the pulse data output signal comprising a duty cycle; an output stage to modulate an output current signal based upon the pulse data output signal; and a duty cycle control circuit, including an ***average power approximation circuit***, to control the duty cycle of the pulse data output signal based, at least in part, on an approximation of an average power of the pulse data output signal. *Emphasis Added.*

Applicants claim (in currently amended claim 7):

> 7. (Currently Amended) A method comprising: generating a pulse data output signal in response to an input signal, the pulse data output signal comprising a duty cycle; and controlling the duty cycle of the pulse data output signal based, at least in part, upon an approximation of the average power of the pulse data output signal, wherein the approximation of the average power is generated using an ***average power approximation circuit***. *Emphasis Added.*

Applicants respectfully assert that the combination of the teaching of Kobayashi and Larson fails to disclose an "***average power approximation circuit***", as claimed in claim 1 and claim 7 of the subject application. Accordingly, applicants respectfully assert that the combination of the teaching of Kobayashi and Larson is not a proper basis for a 35 USC §103(a) rejection, as the combination of the teaching of Kobayashi and Larson fails to disclose each and every element of the applicants' claimed invention.

Concerning the "***average power approximation circuit***" claimed by the applicants, the applicants disclose that:

> An "average power" of a signal as referred to herein relates to the average power transmitted over a time period. A pulse data signal transmitting a high signal

> voltage in pulse periods (e.g., to represent a "one") may transmit an average power that may vary according to a duty cycle associated with a pulse period. Such a pulse data signal, for example, may transmit a higher average power at higher duty cycles and a lower average power at lower duty cycles. However, this is merely an example of how an average power of a signal may be determined and embodiments of the present invention are not limited in this respect. *See Paragraph 0025 of the Subject Application.*
>
> Further, applicants disclose that:
>
> A capacitor 422 may be coupled to a first input terminal of the current steering device 406 and an output terminal of the operational amplifier 416. The capacitor 422 may receive and integrate an amplified signal from the output terminal of the operational amplifier 416 to maintain a voltage at the first input terminal of the current steering device 406 that represents the average power approximation (i.e., of the pulse data output signal). In response to a difference between a voltage at the first input terminal and a reference voltage V.sub.ref at a second input terminal of the current steering device 406, the current steering device 406 may adjust the currents i.sub.a and i.sub.b to adjust or maintain the duty cycle of the pulse data output signal as described above. Accordingly, I/O channels 20, 22 are entities through which data is received from or transmitted to an external system. *See Paragraph 0040 of the Subject Application.*

Kobayashi teaches a laser driver circuit that may provide positive peak control or pre-emphasis (provided by circuit 102 of FIG. 2 or circuit 102' of FIG. 6) and negative peak control or de-emphasis (provided by circuit 104 of FIG. 2 or circuit 104' of FIG. 6). Column 4, lines 19 – 21. The current source I_{CS1} of circuit 102, 102' may provide a weighing factor for the degree of pre-emphasis such that when "the current source Ics1=0, zero pre-emphasis will be implemented. When the current source Ics1 increases, an increasing degree of pre-emphasis will occur." Column 4, lines 38 – 42. Similarly, the current source I_{CS2} of circuit 104, 104' may provide a weighing factor for the degree of de-emphasis such that when "the current source Ics2 =0, zero de-emphasis will occur. When the current source Ics2 is increased, an increasing degree of de-emphasis will occur." Column 5, lines 1 – 3.

The pre-emphasis and de-emphasis may introduce duty cycle distortion seen in Kobayashi's FIGs. 4a and 5a when compared to FIG. 3a. Column 6, lines 42 – 44. Therefore, in the embodiment of FIG. 6, Kobayashi teaches a control circuit 150 "implemented as a duty cycle distortion (DCD) control circuit ***that compensates for the DC offset that may be introduced by the pre-emphasis and de-emphasis circuits 102 and 104.***" (emphasis added). Column 6, lines

60 – 63. The duty cycle distortion control circuit may have the current source I_{DCD} of a set or tuned magnitude to "compensate for the output DC offset produced by the pre-emphasis and de-emphasis circuits 102' and 104'." Column 7, lines 6 – 8. In other words, Kobayashi teaches the duty cycle control circuit 150 is provided to compensate for the amount of DC offset that may be introduced by the pre-emphasis and de-emphasis circuits 102' and 104'.

So not only does Kobayashi not disclose, teach, or suggest "a duty cycle control circuit, including an ***average power approximation circuit***, to control the duty cycle of the pulse data output signal based, at least in part, on an approximation of an average power of the pulse data output signal" as required by claim 1, it actually teaches away from such a limitation by teaching a duty cycle compensation circuit 150 that is provided to compensate for DC offset produced by the pre-emphasis and de-emphasis circuits 102' and 104'. Accordingly, Kobayashi fails to disclose "an approximation of an average power of the pulse data output signal" or an "***average power approximation circuit***" as required by claims 1 and 7 of the subject application.

Further, Larson also fails to disclose "an approximation of an average power of the pulse data output signal" or "an average power approximation circuit" as required by claims 1 and 7 of the subject application. Larson teaches an "apparatus for supplying current to a laser diode." Column 1, lines 10 – 11. In Larson's system of FIG. 1, "the laser diode 4 provides the necessary light in order to read from an electro-optic memory or write upon it." Column 2, lines 55 – 57. Before a read or a write function, a threshold current is drawn through the laser diode 4 by the threshold current source 14 to bring the laser up to the lasing point. For a read function, a combination of current from the threshold current source 14 and the read current source 12 via the read switch 10 is drawn through the laser diode 4. For a write function, a combination of current from the threshold current source 14 and the write current source 16 via the write switch 18 is drawn through the laser diode 4.

Figure 2 of Larson provides details on the read switch 10 of FIG. 1. The read switch 10 includes transistors 20 and 22. In operation, "one transistor is turned on while the other is turned off." Column 4, lines 11 – 12. Schottky diodes 24 and 26 are placed in series with the emitters of the differential pair formed by transistors 20 and 22. "The Schottky diodes block the path back through the off transistor and allow only the current source current to be switched, as the path back through the off-transistor is blocked." Column 4, lines 49 – 53.

Regarding the resistor 28 and capacitor 34 of FIG. 2, Larson teaches:

> The resistor 28 and capacitor 34 connected between the cathodes of the Schottky diodes and the current source provide two functions. First, they provide a long term balancing effect due to the time constant (RC) being relatively long (compared to the 300 MHz switching rate). This is needed because the current source is controlled by current in the laser diode and this current only passes through Q1. Thus there is a possibility that the current through Q1 could become significantly less than the current through Q2 and the closed loop control would not know the difference since laser diode power was correct. However, for this to occur, the voltage drop across Q2 base to emitter and the Schottky diode on the Q2 side would be greater than the corresponding voltage drops on Q1's side of the differential switch. ***The capacitor acts to integrate (average) the voltage at the Schottky diode's cathode and thus prevent the pulse to pulse voltage variations from occurring***. *See Larson, Column 6, lines 12 – 28, emphasis added.*

Accordingly, capacitor 34 helps to prevent pulse to pulse voltage variations that may occur if e.g., the current through transistor Q1 was less than the current though transistor Q2. Accordingly, Larson does not disclose, teach, or suggest "an approximation of an average power of the pulse data output signal" or an "***average power approximation circuit***", as required by claims 1 and 7 of the subject application.

Accordingly, applicants respectfully assert that the combination of the teaching of Kobayashi and Larson is not a proper basis for a 35 USC §103(a) rejection, as the combination of the teaching of Kobayashi and Larson fails to disclose each and every element of applicants' currently amended claims 1 and 7. Therefore, the applicants respectfully assert that independent claims 1 and 7 are patentable over the cited combination of references.

Further, as dependent claims 2-3 directly depend upon independent claim 1, applicants respectfully assert that claims 2-3 are also patentable over the cited combination of references. Additionally, as dependent claim 8 directly depends upon independent claim 7, applicants respectfully assert that claim 8 is also patentable over the cited combination of references.

The Examiner rejects claims 4-6 and 9-11, under 35 USC §103(a), based upon the combination of the teaching of Kobayashi, Larson and Gilliland et al (U.S. Patent No.: 6,711,189, hereinafter Gilliland).

For the reasons discussed above, applicants respectfully assert that the combination of Kobayashi and Larson fails to disclose, teach, or suggest "an approximation of an average

power of the pulse data output signal" or an "***average power approximation circuit***", as required by claims 1 and 7 of the subject application.

As dependent claim 4-6 depend (either directly or indirectly) upon independent claim 1, and dependent claim 9-11 depend (either directly or indirectly) upon independent 7, the applicants respectfully assert that claims 4-6 and 9-11 are also patentable over the cited combination of references.

The Examiner rejects claim 12, under 35 USC §103(a), based upon the combination of the teaching of Kobayashi, Larson and Kenny (U.S. Patent No.: 6,654,565, hereinafter Kenny). Specifically, the Examiner relies on Kenny to disclose "a communication system utilizing a serializer".

Applicants claim (in currently amended claim 12):

> 12. (Currently Amended) A system comprising: a serializer to provide a serial data signal in response to a parallel data signal; a laser device adapted to be coupled to an optical transmission medium to transmit an optical signal in the optical transmission medium in response to a current signal; and a laser driver circuit comprising: an input stage to receive an input signal; a limiting amplifier to generate a pulse data output signal in response to the input signal, the pulse data output signal comprising a duty cycle; an output stage to modulate the current signal based upon the pulse data output signal; and a duty cycle adjustment circuit, including an ***average power approximation circuit***, to adjust the duty cycle of the pulse data output signal based, at least in part, on an approximation of an average power of the pulse data output signal.

For the reasons discussed above, applicants respectfully assert that the combination of Kobayashi and Larson fails to disclose, teach, or suggest "an approximation of an average power of the pulse data output signal" or an "***average power approximation circuit***", as required by claim 12 of the subject application. As Kenny also fails to disclose, teach, or suggest "an approximation of an average power of the pulse data output signal" or an "***average power approximation circuit***", the applicants respectfully assert that the combination of the teaching of Kobayashi, Larson and Kenny is not a proper basis for a 35 USC §103(a) rejection, as the combination of the teaching of Kobayashi, Larson and Kenny fails to disclose each and every element of applicants' currently amended claim 12. Therefore, the applicants respectfully assert that independent claim 12 is patentable over the cited combination of references.

The Examiner rejects claims 13-17, under 35 USC §103(a), based upon the combination of the teaching of Kobayashi, Larson and Diaz et al (U.S. Patent No.: 6,822,987, hereinafter Diaz).

For the reasons discussed above, applicants respectfully assert that the combination of Kobayashi, Larson and Kenny fails to disclose, teach, or suggest "an approximation of an average power of the pulse data output signal" or an "***average power approximation circuit***", as required by claim 12 of the subject application.

As dependent claims 13-17 depend (either directly or indirectly) upon independent claim 12, the applicants respectfully assert that claims 13-17 are also patentable over the cited combination of references.

The Examiner provisionally rejects claims 12-17 based on an assertion of obviousness-type double patenting as being unpatentable over claims 1-6 of co-pending Application No. 10,422,829 in view of Kobayashi and Larson.

Pursuant to a telephonic discussion on 25 January 2006 between Examiner Tod Van Roy and Attorney Brian J. Colandreo, it was agreed that the provisional obviousness-type double patenting rejection shall be stayed pending the outcome of co-pending Application No. 10,422,829. At that time, if the Examiner believes that the claims of co-pending Application No. 10,422,829 still read on the claims of the subject application, a terminal disclaimer will be discussed and considered.

No new matter has been added by these amendments. While the applicants respectfully assert that the subject application is now in condition for allowance, the Examiner is invited to telephone applicants' attorney (603-668-6560) to facilitate prosecution of this application. Please apply any charges or credits to deposit account 50-2121.

Respectfully submitted,

MAGOON ET AL.

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Attachment

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop AF, Commissioner of Patents, P.O.Box 1450, Alexandria, VA 22313-1450, on this 25 day of January, 2006.

Valerie Borry _____ Valerie Borry

Name Signature